IN THE CLAIMS

Please amend the claims to read as indicated herein.

Please cancel claim 4.

1. (currently amended) A circuit for providing a pulse to drive a capacitive load, said circuit comprising:

a first inductive component that influences both a transition time of a rising edge of said pulse and a transition time of a falling edge of said pulse; and

a second inductive component that influences one of said transition time of said rising edge and said transition time of said falling edge so that said rising edge and said falling edge are asymmetrical

wherein said capacitive load is a panel capacitance in a plasma display panel.

2. (original) The circuit of claim 1,

wherein said circuit is characterized by (a) a first current that flows through said first inductive component to produce one of said rising edge and said falling edge, and (b) a second current that flows through said first inductive component and said second inductive component in series to produce the other of said rising edge and said falling edge, and

wherein said circuit further comprises:

a first switching device for enabling and disabling a path for said first current; and

a second switching device for enabling and disabling a path for said second current.

3. (original) The circuit of claim 1,

wherein said circuit is characterized by (a) a first current that flows through said first inductive component to produce one of said rising edge and said falling edge, and (b) a second current that flows through said first inductive component and said second inductive component in parallel to produce the other of said rising edge and said falling edge, and

wherein said circuit further comprises:

a first switching device for enabling and disabling a path for said first current; and

a second switching device for enabling and disabling a path for said second current.

4. (canceled)

5. (original) The circuit of claim 1, further comprising:

a switching device connectable to said capacitive load, for enabling and disabling a path from a voltage supply to said capacitive load; and

a controller, responsive to a signal derived from said first inductive component, for controlling said switching device,

wherein said controller controls said switching device to enable said path when a current flow through said first inductive component approaches zero.

6. (original) The circuit of claim 1, further comprising:

a switching device connectable to said capacitive load, for enabling and disabling a path from a node of common potential to said capacitive load; and

a controller responsive to a signal derived from said first inductive component, for controlling said switching device,

wherein said controller controls said switching device to enable said path when a current flow through said first inductive component approaches zero.

7. (original) The circuit of claim 1, further comprising:

a switching device connectable to said capacitive load, for enabling and disabling a path from a voltage supply to said capacitive load; and

a controller responsive to a signal derived from said second inductive component, for controlling said switching device,

wherein said controller controls said switching device to enable said path when a current flow through said second inductive component approaches zero.

8. (original) The circuit of claim 1, further comprising:

a switching device connectable to said capacitive load, for enabling and disabling a conductive path from a node of common potential to said capacitive load; and

a controller responsive to a signal derived from said second inductive component, for controlling said switching device,

wherein said controller controls said switching device to enable said conductive path when a current flow through said second inductive component approaches zero.

9. (original) A circuit for providing a sustain pulse to drive a capacitive load in a plasma display panel, said circuit comprising:

a first inductor;

a second inductor;

a first transistor for enabling and disabling a path for a first current through said first inductor to produce a rising edge of said pulse;

a second transistor for enabling and disabling a path for a second current through said first inductor and said second inductor in series to produce a falling edge of said pulse;

wherein said rising edge and said falling edge are asymmetrical.

10. (original) The circuit of claim 9, further comprising a third transistor connectable to said capacitive load, for enabling and disabling a path from a voltage supply to said capacitive load.

11. (original) The circuit of claim 10, further comprising a controller responsive to a signal derived from said first inductor, for controlling said third transistor, wherein said controller controls said third transistor to enable said path when a current flow through said first inductor approaches zero.

12. (original) The circuit of claim 10, further comprising a controller responsive to a signal derived from said second inductor, for controlling said third transistor, wherein said controller controls said third transistor to enable said path when a current flow through said second inductor approaches zero.

13. (original) The circuit of claim 9, further comprising a third transistor connectable to said capacitive load, for enabling and disabling a path from a node of common potential to said capacitive load.

14. (original) The circuit of claim 13, further comprising a controller responsive to a signal derived from said first inductor, for controlling said third transistor, wherein said controller controls said third transistor to enable said path when a current flow through said first inductor approaches zero.

15. (original) The circuit of claim 13, further comprising a controller responsive to a signal derived from said second inductor, for controlling said third transistor, wherein said controller controls said third transistor to enable said path when a current flow through said second inductor approaches zero.

16. (original) A circuit for providing a driving pulse to a display panel having panel electrodes and panel capacitance, said circuit comprising:

a first inductor that influences both a transition time of a rising edge of said pulse and a transition time of a falling edge of said pulse, said first inductor having a first terminal and a second terminal, said second terminal connectable to said panel electrodes;

a driving voltage source for providing a driving voltage referenced to a common potential;

a voltage supply for providing a supply voltage referenced to said common potential, wherein said supply voltage is of a magnitude that is greater than said driving voltage;

a first switching device for enabling and disabling a conductive path from said driving voltage source to said first terminal in response to an input signal transition, said input signal transition commencing a first state wherein, during an enabling of said conductive path, a current flow occurs through said first inductor to charge said panel capacitance, said first inductor causing said panel electrodes to achieve a voltage magnitude in excess of said driving voltage, prior to said current flow reaching zero;

a second switching device, connectable to said panel electrodes, for enabling and disabling a conductive path from said voltage supply to said second terminal and said panel electrodes;

a switch control coupled to said first inductor and responsive to said current flow therein, said switch control operative during at least a portion of said first state to control said second switching device to disable conduction therethrough, and thereafter in response to a signal derived from said first inductor, to control said second switching device to enable conduction therethrough a time prior to said current flow reaching zero, whereby said voltage supply means, during a succeeding second state, supplies current to both said panel electrodes and flyback current to said first inductor; and

a second inductor that influences one of said transition time of said rising edge and said transition time of said falling edge so that said rising edge and said falling edge are asymmetrical.